SYLLABUS

(REGULATIONS 2019)

FOR

UNDER GRADUATE PROGRAMMES
CHOICE BASED CREDIT SYSTEM

(Applicable to the students admitted from the Academic Year 2019-20 onwards)

B.E. – ELECTRONICS AND COMMUNICATION ENGINEERING

EASWARI ENGINEERING COLLEGE
(AUTONOMOUS INSTITUTION)
Bharathi Salai, Ramapuram, Chennai – 600 089

191ECC601T VLSI DESIGN **L T P R C 0**
3 0 0 3

PREREQUISITES: NIL

COURSE OBJECTIVES:

- Study the fundamentals of CMOS circuits and its characteristics.
- Learn the design and realization of combinational & sequential digital circuits.
- Architectural choices and performance tradeoffs involved in designing and realizing the circuits in CMOS technology
- Learn the different FPGA architectures and testability of VLSI circuits

UNIT I : INTRODUCTION TO MOS TRANSISTOR 9

MOS Transistor Theory, Long-Channel I-V Charteristics - CMOS Inverter, CMOS Fabrication, Layout Design Rules, Stick Diagrams, CV Characteristics, Non ideal I-V Effects, DC Transfer characteristics, Scaling principles and fundamental limits, Device Modeling in SPICE

UNIT II : COMBINATIONAL LOGIC CIRCUIT DESIGN 9

Circuit Families: Static CMOS, Ratioed Circuits, Cascode Voltage Switch Logic, Dynamic CMOS, Pass Transistor Logic, Complementary Pass Transistor Logic, Transmission Gates, Domino, Dual Rail Domino, Differential Cascode Voltage Switch with Pass-Gate (DCVSPG) Power: Static Power and Dynamic Power Low Power Architecture.

UNIT III : SEQUENTIAL LOGIC CIRCUIT DESIGN 9

Timing Metrics for Sequential Circuits, Static Latches and Registers, Dynamic Latches and Registers, Pulse Registers, Sense-Amplifier Based Registers, Pipelining: An approach to optimize sequential circuits Timing Issues: Timing Classification Of Digital System, Synchronous Design.

UNIT IV : DESIGN OF ARITHMETIC BUILDING BLOCKS AND SUBSYSTEM 9

Arithmetic Building Blocks: Datapaths in Digital Processor Architectures, Adders, Multipliers, Shifters, Power and Speed tradeoffs, Designing Memory and Array structures: Memory Architectures and Building Blocks, Memory Core, Memory Peripheral Circuitry.

UNIT V : IMPLEMENTATION STRATEGIES AND TESTING 9

Full custom and Semi-custom design, Standard cell design and cell libraries, FPGA building block architectures, FPGA Interconnect Routing Procedures. Design for Testability: Ad Hoc Testing, Scan Design, BIST, IDDQ Testing, Design for Manufacturability, Boundary Scan.

TOTAL PERIODS: 45

HOURS COURSE OUTCOMES:

Upon completion of this course, student will be able to:

- Analyze the characteristics of MOS transistors
- Design the combinational and sequential logic circuits using MOSFET
- Implement the VLSI circuits with power and timing strategies
- Apply the VLSI concepts in arithmetic building blocks and memory subsystems.
- Assess the nomenclature and technology of FPGA devices and VLSI testing methods
- Test the VLSI Circuits at chip and board levels

TEXT BOOKS:

1. Jan M. Rabaey, Anantha Chandrakasan, Borivoje. Nikolic, “Digital Integrated Circuits: A Design perspective”, Second Edition , Pearson , 2016.(UNIT II III,IV)

2. Neil H.E. Weste, David Money Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”, 4th Edition, Pearson, 2017 (UNIT I,V)

REFERENCE BOOKS:

1. R.Jacob Baker, Harry W.LI., David E.Boyee, “CMOS Circuit Design, Layout and Simulation”, Prentice Hall of India 2005.
2. Smith M.J., “Application Specific Integrated Circuits”, Addison Wesley, 1997
3. Sung-Mo kang, Yusuf leblebici, Chulwoo Kim, “CMOS Digital Integrated Circuits:Analysis&Design” ,4th edition McGraw Hill Education,2013
4. Wayne Wolf, “Modern VLSI Design: System On Chip”, Pearson Education, 2007

E-BOOKS / WEB REFERENCES:

1. https://onlinecourses.nptel.ac.in/noc20_ee29/course

191ECC602T	**ANTENNAS AND MICROWAVE ENGINEERING**	**L**	**T**	**P**	**R**	**C**	**0**
		3	**0**	**0**		**3**	

PREREQUISITES: NIL

COURSE OBJECTIVES:

- To enable the student to understand the basic principles in antenna and microwave system design
- To enhance the student knowledge in the area of various antenna designs.
- To enhance the student knowledge in the area of microwave components and antenna for practical applications

UNIT I : INTRODUCTION TO MICROWAVE SYSTEMS AND ANTENNAS **9**

Microwave frequency bands, Physical concept of radiation, Near- and far-field regions, Fields and Power Radiated by an Antenna, Antenna Pattern Characteristics, Antenna Gain and Efficiency, Aperture

Efficiency and Effective Area, Antenna Noise Temperature and G/T, Impedance matching, Friis transmission equation, Link budget and link margin, Noise Characterization of a microwave receiver.

UNIT II : RADIATION MECHANISMS AND DESIGN ASPECTS 9

Radiation Mechanisms of Linear Wire and Loop antennas, Aperture antennas, Reflector antennas, Microstrip antennas and Frequency independent antennas, Design considerations and applications

UNIT III : ANTENNA ARRAYS AND APPLICATIONS 9

Two-element array, Array factor, Pattern multiplication, Uniformly spaced arrays with uniform and non-uniform excitation amplitudes, Smart antennas.

UNIT IV : PASSIVE AND ACTIVE MICROWAVE DEVICES 9

Microwave Passive components: Directional Coupler, Power Divider, Magic Tee, attenuator, resonator, Principles of Microwave Semiconductor Devices: Gunn Diodes, IMPATT diodes, Schottky Barrier diodes, PIN diodes, Microwave tubes: Klystron, TWT, Magnetron.

UNIT V : MICROWAVE DESIGN PRINCIPLES 9

Impedance transformation, Impedance Matching, Microwave Filter Design, RF and Microwave Amplifier Design, Microwave Power amplifier Design, Low Noise Amplifier Design, Microwave Mixer Design, Microwave Oscillator Design

TOTAL PERIODS: 45 HOURS

COURSE OUTCOMES:

Upon completion of this course, student will be able to:

- Apply the fundamentals of antennas and compute the related performance metrics.
- Analyze the radiation mechanisms of wire, microstrip, reflector and frequency independent antennas.
- Design antenna arrays and smart antennas for real time applications.
- Implement the concept of active and passive components in microwave devices and tubes.
- Construct microwave amplifier and oscillator for high frequency applications.

TEXT BOOKS:

1. David M. Pozar, "Microwave Engineering", Fourth Edition, Wiley India, 2012. (UNIT I,IV,V)
2. John D Krauss, Ronald J Marhefka and Ahmad S. Khan, "Antennas and Wave Propagation" Fourth Edition, Tata McGraw-Hill, 2006. (UNIT I, II, III)

REFERENCE BOOKS:

1. Collin R.E., "Foundations for Microwave Engineering", Second edition, IEEE Press, 2001
2. Constantine A. Balanis, "Antenna Theory Analysis and Design", Third edition, John Wiley India Pvt Ltd., 2005.

191ECC603T **INTERNET OF THINGS** **L T P R C 0**
3 0 0 3

PREREQUISITES: NIL

COURSE OBJECTIVES:

- To understand the basics of Internet of Things
- To get an idea of some of the application areas where Internet of Things can be applied
- To understand the middleware for Internet of Things
- To understand the concepts of Web of Things

- To understand the concepts of Cloud of Things with emphasis on Mobile cloud computing
- To understand the IOT protocols

UNIT I : INTRODUCTION **10**

Definitions and Functional Requirements –Motivation – Architecture - Web 3.0 View of IoT– Ubiquitous IoT Applications – Four Pillars of IoT – DNA of IoT - The Toolkit Approach for End-user Participation in the Internet of Things. Middleware for IoT: Overview – Communication middleware for IoT –IoT Information Security.

UNIT II : IOT PROTOCOLS **8**

Protocol Standardization for IoT – Efforts – M2M and WSN Protocols – SCADA and RFID Protocols – Issues with IoT Standardization – Unified Data Standards – Protocols – IEEE 802.15.4 – BACNet Protocol – Modbus – KNX – Zigbee Architecture – Network layer – APS layer – Security.

UNIT III : WEB OF THINGS **9**

Web of Things versus Internet of Things – Two Pillars of the Web – Architecture Standardization for WoT– Platform Middleware for WoT – Unified Multitier WoT Architecture – WoT Portals and Business Intelligence. Cloud of Things: Grid/SOA and Cloud Computing – Cloud Middleware – Cloud Standards – Cloud Providers and Systems – Mobile Cloud Computing – The Cloud of Things Architecture.

UNIT IV : INTEGRATED SYSTEMS **9**

Integrated Billing Solutions in the Internet of Things Business Models for the Internet of Things - Network Dynamics: Population Models – Information Cascades - Network Effects - Network Dynamics: Structural Models - Cascading Behavior in Networks - The Small-World Phenomenon

UNIT V : APPLICATIONS **9**

The Role of the Internet of Things for Increased Autonomy and Agility in Collaborative Production Environments - Resource Management in the Internet of Things: Clustering, Synchronisation and Software Agents. Applications - Smart Grid – Electrical Vehicle Charging.

TOTAL PERIODS: 45

HOURS COURSE OUTCOMES:

Upon completion of this course, student will be able to:

- Examine the basic elements and functional Requirements of Internet of Things
- Illustrate the various protocols for Internet of Things
- Design business intelligence and information security for WoT
- Analyze the different business models for network dynamics
- Develop an IoT application based on the real time scenarios
- Determine the Role of the Internet of Things for Increased Autonomy and Agility in Collaborative Production Environments - Resource Management

TEXT BOOKS:

1. David Easley and Jon Kleinberg, “Networks, Crowds, and Markets: Reasoning About a Highly Connected World”, Cambridge University Press - 2010
2. Dieter Uckelmann; Mark Harrison; Florian Michahelles, “Architecting the Internet of Things”, Springer – 2011
3. Honbo Zhou, “The Internet of Things in the Cloud: A Middleware Perspective”, CRC Press – 2012

REFERENCE BOOKS:

1. Olivier Hersent, David Boswarthick, Omar Elloumi , “The Internet of Things – Key applications and Protocols”, Wiley, 2012
2. Olivier Hersent , Omar Elloumi and David Boswarthick , “The Internet of Things: Applications to the Smart Grid and Building Automation”, Wiley -2012

191ECC611L VLSI DESIGN LABORATORY **L T P R C 3**
0 0 1 2

PREREQUISITES: NIL

COURSE OBJECTIVES:

- To learn Hardware Descriptive Language(Verilog/VHDL)
- To learn the fundamental principles of VLSI circuit design in digital and analog domain
- To familiarize fusing of logical modules on FPGAs
- To provide hands on design experience with professional design EDA platforms

LIST OF EXPERIMENTS

Part I: Design the following Digital System using HDL &Implement by Xilinx/Altera FPGA (36 Periods)

1. Adder – Ripple Carry Adder/ Carry Lookahead Adder (Minimum 8 Bit)
2. Multiplier – Booth Multiplier/ Wallace Tree Multiplier/Array Multiplier (4 Bit Minimum)
3. Comparators, Decoders, Multiplexers and Demultiplexers
4. Arithmetic & Logic Unit (4 bit Minimum)
5. Latches & Flip-Flops
6. Universal Shift Register (4 bit Minimum)
7. Synchronous Counters (4 bit)
8. Finite State Machine (Moore/Mealy)
9. Random Access Memory(4X4)

Requirements for Part I: Xilinx ISE/Altera Quartus/ equivalent EDA Tools along with Xilinx/Altera/equivalent FPGA Boards

Part-II Analog Circuit Design (24 Periods)

10. Design and Simulate a CMOS Inverter by performing Schematic Simulations.
11. Design and simulate simple 5 transistor differential amplifier. Analyze Gain, Bandwidth and CMRR by performing Schematic Simulations.

12. Design, Simulate and Extract the layout ofa CMOS Inverter

Requirements for Part II : Cadence/Synopsis/ Mentor Graphics/Tanner/equivalent EDA Tools

TOTAL PERIODS: 60

HOURS COURSE OUTCOMES:

Upon completion of this course, student will be able to:

- Model a digital circuit using Verilog HDL and validate its functionality
- Import the logic modules into FPGA Boards
- Analyse the VLSI entities from synthesis report
- Simulate a CMOS circuit in Transistor level
- Analyze Gain, Bandwidth and CMRR of Differential amplifier by performing Schematic Simulations
- Develop the layout for CMOS circuit designs in GDS II file format

191ECE603T DIGITAL IMAGE PROCESSING **L T P R C 0 0 3 0 3**

PREREQUISITES: NIL

COURSE OBJECTIVES:

- Understand the digital image fundamentals.
- Analyze the image enhancement techniques.
- Understand the image restoration techniques.
- Familiarize the image compression techniques
  Understand the image segmentation and representation techniques.

UNIT I : DIGITAL IMAGE FUNDAMENTALS **9**

Introduction – Origin – Steps in Digital Image Processing – Components – Elements of Visual Perception – Image Sensing and Acquisition –

Image Sampling and Quantization – Relationships between pixels – color fundamentals and models.

UNIT II : IMAGE ENHANCEMENT 9

Spatial Domain: Gray level transformations – Histogram processing – Basics of Spatial Filtering–Smoothing and Sharpening Spatial Filtering – Frequency Domain: Introduction to Fourier Transform – Smoothing and Sharpening frequency domain filters – Ideal, Butterworth and Gaussian filters- Homomorphic filtering.

UNIT III : IMAGE RESTORATION 9

Introduction to degradation-Types of image degradations-Image degradation model- Noise models – Mean Filters – Order Statistics Filters– Band reject Filters – Band pass Filters – Notch Filters – Image Restoration Technique - Inverse Filtering – Wiener filtering –Blind Image Restoration. Morphological processing- erosion and dilation.

UNIT IV : IMAGE COMPRESSION 9

Compression: Fundamentals – Image Compression models – Lossless Compression Algorithms - Lossless Predictive Coding – Lossy Compression Algorithms- Lossy Predictive Coding -Block Transform Coding – Compression Standards: JPEG – JPEG 2000-
MPEG

UNIT V : IMAGE SEGMENTATION AND REPRESENTATION 9

Segmentation: Detection of Discontinuities–Point, Line and Edge detection- Gradient operators- Thresholding – Region based segmentation- Boundary Representation Schemes – Chain Code – Polygonal approximation, signatures – Boundary descriptors – Basic boundary descriptors - Shape number – Regional Descriptors- Patterns and Pattern classes – Recognition based on matching

TOTAL PERIODS: 45 HOURS

COURSE OUTCOMES:

Upon completion of this course, student will be able to:

- Understand the digital Image fundamentals

- Analyze the image enhancement techniques
- Understand the image restoration techniques.
- Familiarize the image compression techniques.
- Understand the Image segmentation and representation techniques.
- Learn to apply image processing techniques in real time applications

TEXT BOOKS:

1. Rafael C. Gonzales, Richard E. Woods, “Digital Image Processing”, Third Edition, Pearson Education, 2010

REFERENCE BOOKS:

1. Malay K. Pakhira, “Digital Image Processing and Pattern Recognition”, First Edition, PHI Learning Pvt. Ltd., 2011.
2. Rafael C. Gonzalez, Richard E. Woods, Steven L. Eddins, “Digital Image Processing Using MATLAB”, Third Edition Tata Mc Graw Hill Pvt. Ltd., 2011.
3. S.Sridhar, “Digital Image Processing”, Second Edition, Oxford University Press, 2016..
4. Willliam K Pratt, “Digital Image Processing”, John Willey, 2002.

191CSE621T	**COMPUTER ARCHITECTURE AND ORGANIZATION**	**L**	**T**	**P**	**R**	**C**	**0**
		3	**0**	**0**		**3**	

PREREQUISITES: NIL

COURSE OBJECTIVES:

- To make students understand the basic structure and operation of digital computer

- To familiarize with implementation of fixed point and floatingpoint arithmetic operations

  To study the design of data path unit and control unit for processor
- To understand the concept of various memories and interfacing
- To introduce the parallel processing technique

UNIT I : COMPUTER ORGANIZATION & INSTRUCTIONS 9

Basics of a computer system: Evolution, Ideas, Technology, Performance, Power wall, Uniprocessors to Multiprocessors. Addressing and addressing modes. Instructions: Operations and Operands, Representing instructions, Logical operations, control operations.

UNIT II : ARITHMETIC OPERATIONS 9

Fixed point Addition, Subtraction, Multiplication and Division. Floating Point arithmetic, High performance arithmetic, Subword parallelism

UNIT III : THE PROCESSOR 9

Introduction, Logic Design Conventions, Building a Datapath - A Simple Implementation scheme - An Overview of Pipelining - Pipelined Datapath and Control. Data Hazards: Forwarding versus Stalling, Control Hazards, Exceptions, Parallelism via Instructions.

UNIT IV : MEMORY AND I/O ORGANIZATION 9

Memory hierarchy, Memory Chip Organization, Cache memory, Virtual memory. Parallel Bus Architectures, Internal Communication Methodologies, Serial Bus Architectures, Mass storage, Input and Output Devices.

UNIT V : ADVANCED COMPUTER ARCHITECTURE 9

Parallel processing architectures and challenges, Hardware multithreading, Multicore and shared memory multiprocessors, Introduction to Graphics Processing Units, Clusters and Warehouse scale computers - Introduction to Multiprocessor network topologies.

TOTAL PERIODS: 45 HOURS

COURSE OUTCOMES:

Upon completion of this course, student will be able to:

- Analyze the processor architecture, addressing modes and instructions.
- Design the arithmetic units for computer architecture.
- Implement the concept of pipelining in the processor.
- Interpret the memories and bus architectures for the processor.
- Develop the multi-core processor based applications using advanced architecture.

TEXT BOOKS:

1. David A. Patterson and John L. Hennessey, “Computer Organization and Design”, Fifth edition, Morgan Kauffman / Elsevier, 2014. (UNIT I-V)
2. Miles J. Murdocca and Vincent P. Heuring, “Computer Architecture and Organization: An Integrated approach”, Second edition, Wiley India Pvt Ltd, 2015 (UNIT IV,V)

REFERENCE BOOKS:

1. Carl Hamacher V, Zvonko G. Varanesic and Safat G. Zaky, “Computer Organization”, Fifth edition, Mc Graw-Hill Education India Pvt Ltd, 2014.
2. Govindarajalu, “Computer Architecture and Organization, Design Principles and Applications", Second edition, McGrawHill Education India Pvt Ltd, 2014.
3. William Stallings “Computer Organization and Architecture”, Seventh Edition, Pearson Education, 2006.

1.
2. Jonathan W.Valvano, “Embedded Microcomputer Systems Real Time Interfacing”, Third Edition Cengage Learning, 2012.

3. Krishna C.M., Kang G. Shin, “Real-Time Systems”,
International Editions, Mc Graw Hill 1997
4. Raymond J.A. Buhr, Donald L.Bailey, “An Introduction to RealTime Systems- From Design to Networking with C/C++”, Prentice Hall, 1999.
5. Sriram V Iyer, Pankaj Gupta, “Embedded Real Time Systems Programming”, Tata Mc Graw Hill, 2004.